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FIG. 1A PRIOR ART

FIRST GENERATION
 SINGLE CPU - MULTIPLE LINE CARDS
 SINGLE ELECTRICAL BACKPLANE

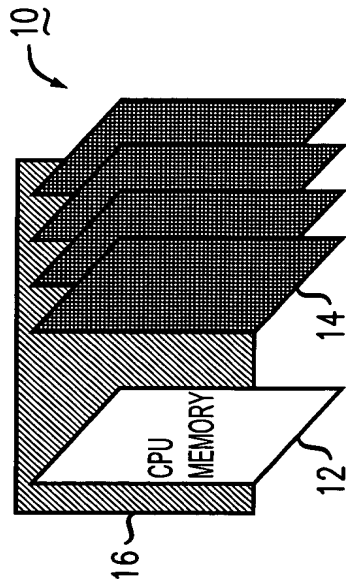


FIG. 1B PRIOR ART

SECOND GENERATION
 ONE CPU PER LINE CARD
 CENTRAL CONTROLLER FOR ROUTING PROTOCOLS

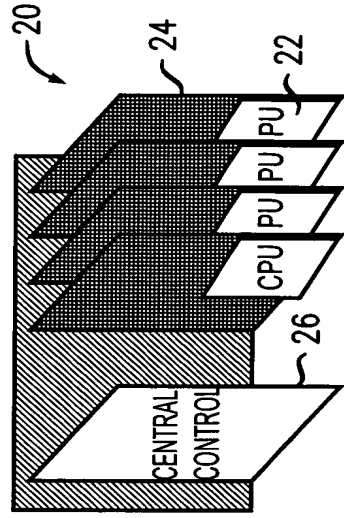


FIG. 1C PRIOR ART

THIRD GENERATION
 ONE CPU PER LINE CARD CENTRAL
 CONTROLLER FOR ROUTING PROTOCOLS
 SWITCH FABRIC FOR INTER-CONNECTION

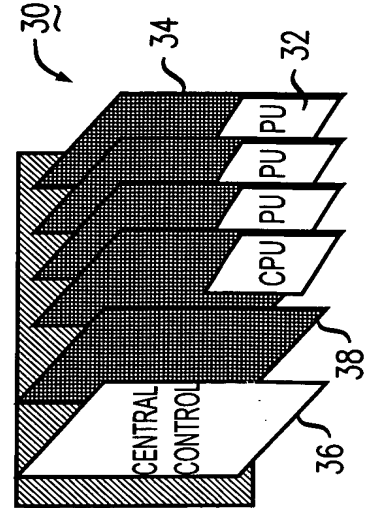
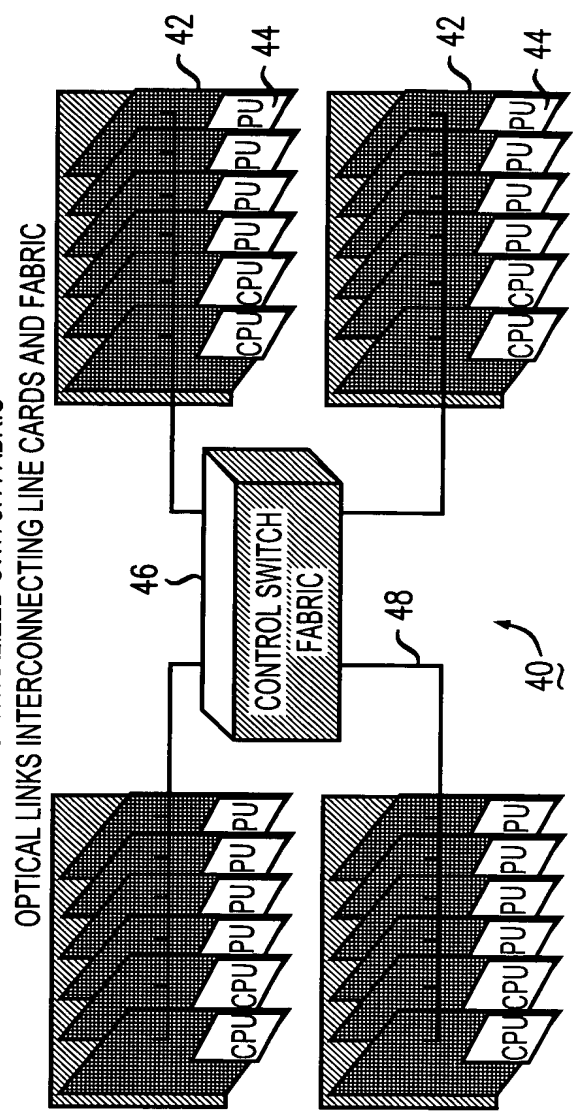


FIG. 1D PRIOR ART

FOURTH GENERATION
 MULTIPLE SHELVES OF LINE CARDS
 CENTRALIZED SWITCH FABRIC
 OPTICAL LINKS INTERCONNECTING LINE CARDS AND FABRIC



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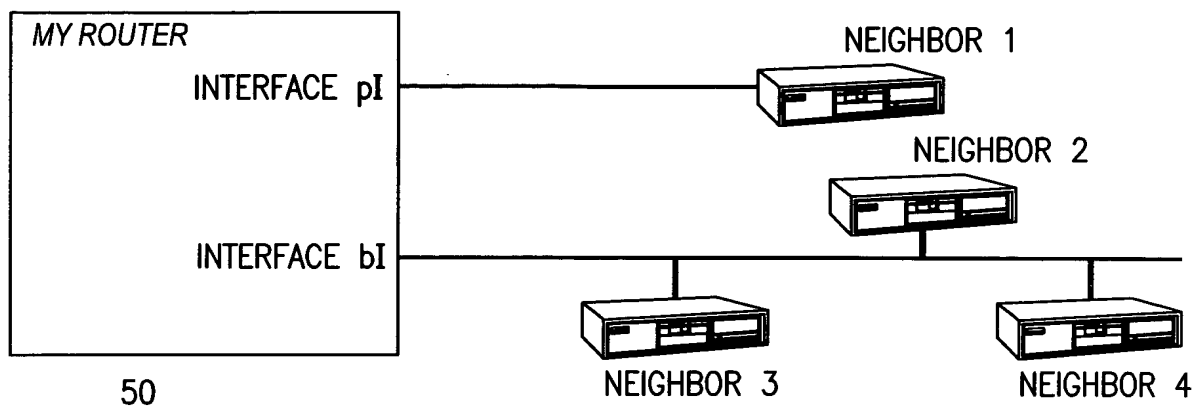


FIG. 2
PRIOR ART

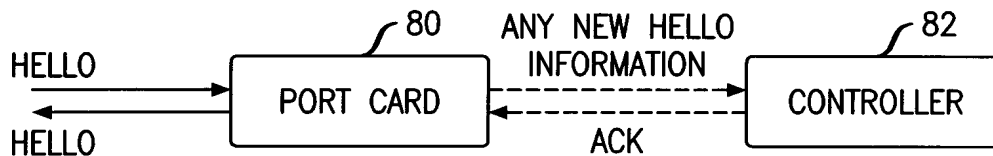


FIG. 5
DISTRIBUTED HELLO PROCESSING

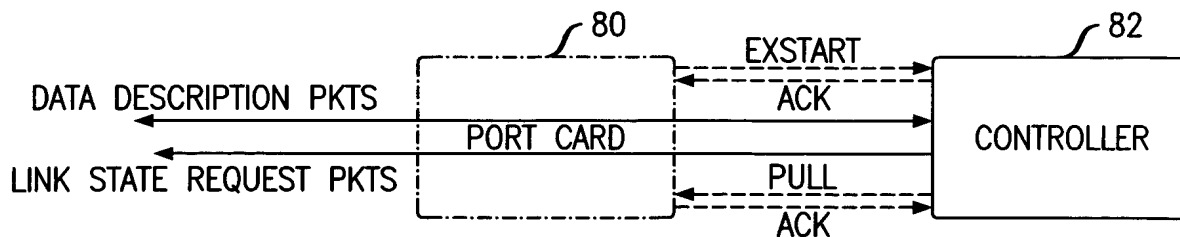


FIG. 6
INITIAL DB EXCHANGE

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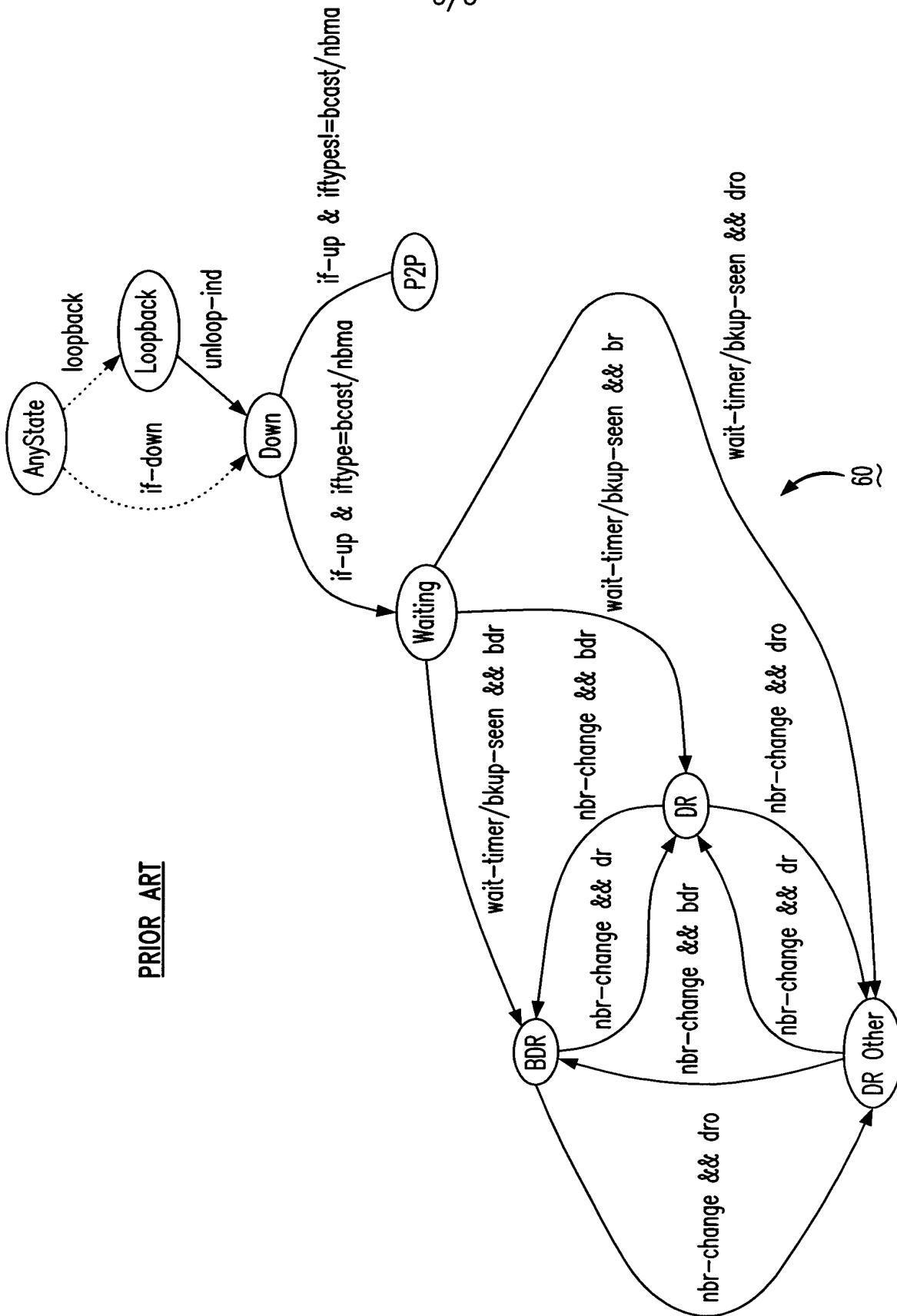


FIG. 3
 OSPF INTERFACE FSM

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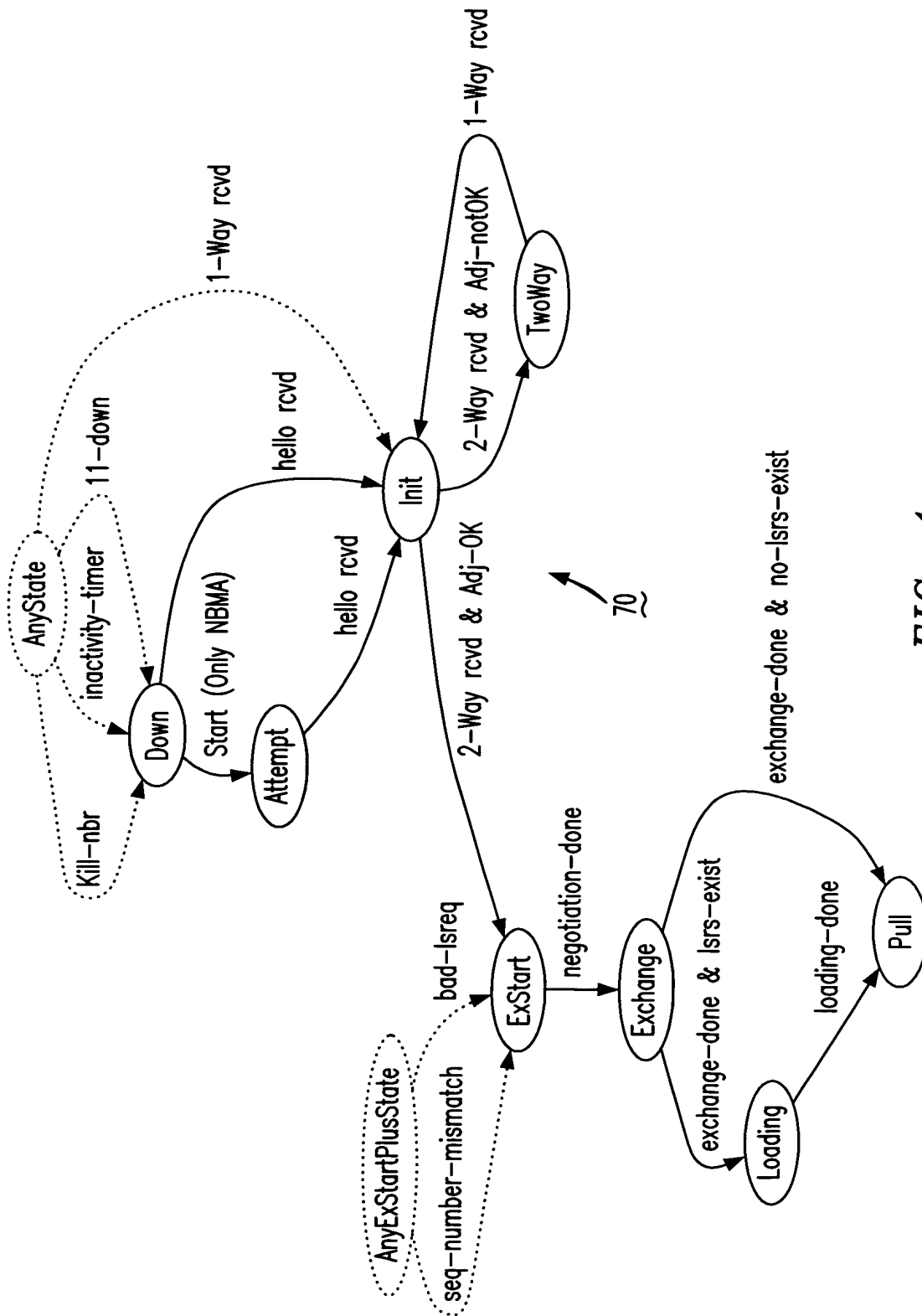


FIG. 4
PRIOR ART

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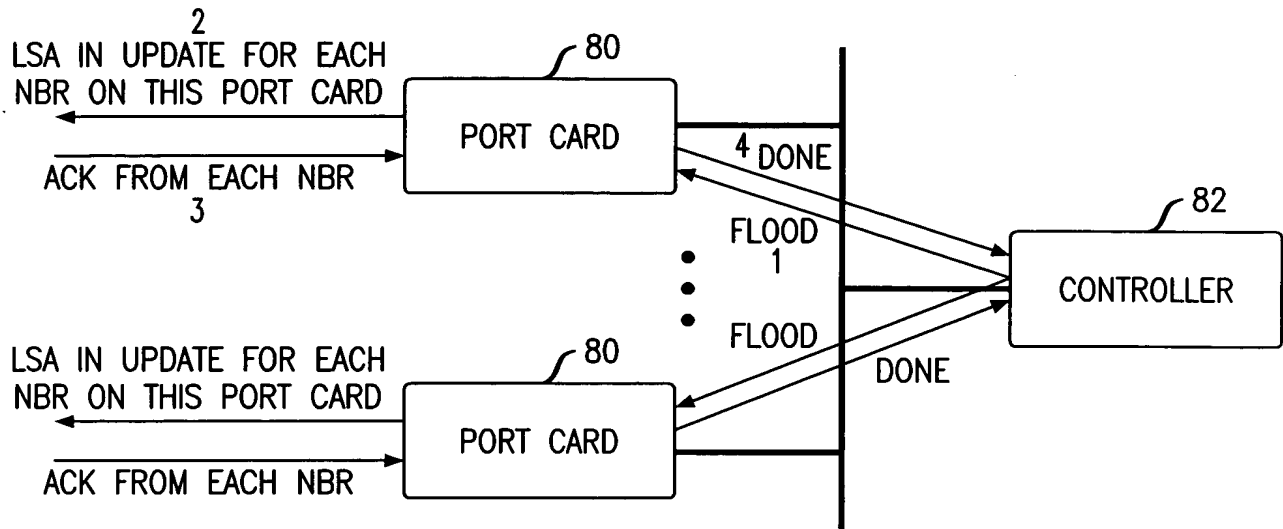


FIG. 7

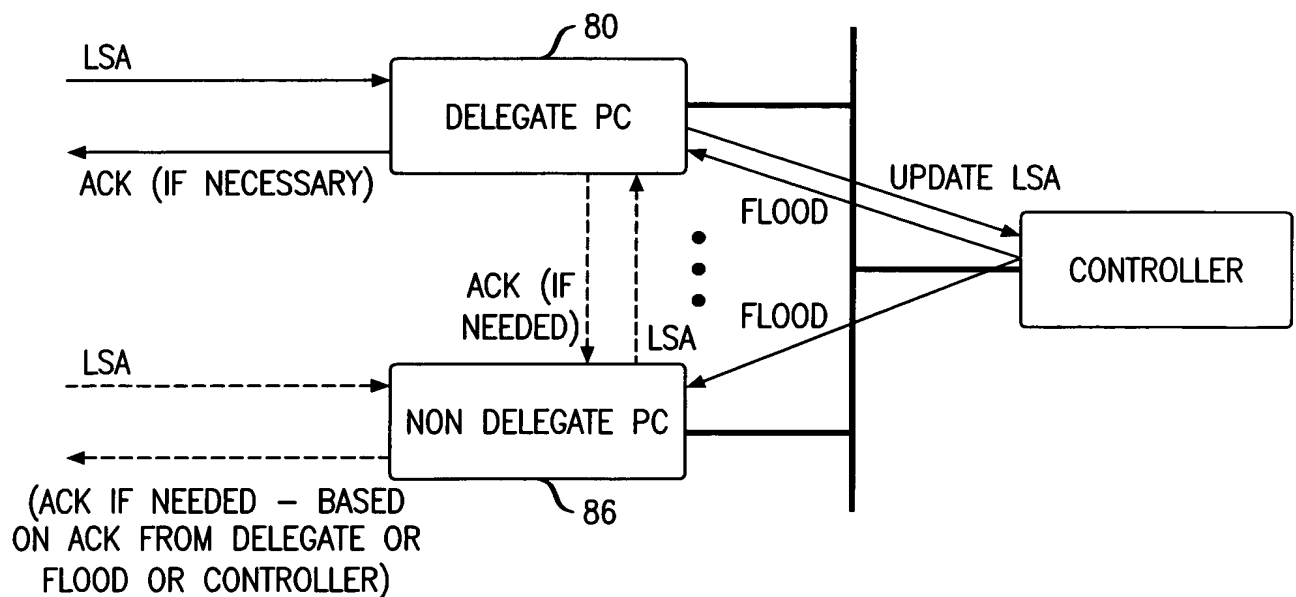


FIG. 8

DISTRIBUTED PROCESSING OF INCOMING LSA UPDATES